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PATENT APPLICATION

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: Yuanlong Wang

Application No.: 09/750,629 **Group No.:** 2112

Filed: 12/28/2000 **Examiner:** Huynh, Kim T.

For: CROSSBAR INTEGRATED CIRCUIT WITH PARALLEL CHANNELS FOR A COMMUNICATION DEVICE

MAIL STOP APPEAL BRIEF - PATENTS
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BRIEF ON APPEAL

INTRODUCTION

Pursuant to the provisions of 37 CFR § 41.31 *et seq.*, Applicants hereby appeal to the Board of Patent Appeals and Interferences (the "Board") from the Examiner's final rejection dated June 24, 2005.

A Notice of Appeal is being concurrently filed with this Appeal Brief. The notice of Appeal is accompanied by the requisite fee per 37 CFR § 41.20(b)(1) and the Appeal Brief is accompanied by the requisite fee per 37 CFR § 41.20(b)(2).

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REAL PARTY IN INTEREST

The entire interest in the present application has been assigned to Conexant Systems, Inc., as recorded at Reel 014546, Frame 0305.

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RELATED APPEALS AND INTERFERENCES

There are no related appeals or interferences.

STATUS OF CLAIMS

Claims 21-40 (all claims) are pending.

Claims 21-40 have been finally rejected.

Claims 21-40 are on appeal.

STATUS OF AMENDMENTS

There are no pending amendments.

SUMMARY OF CLAIMED SUBJECT MATTER

This invention relates generally to a communication circuit that includes a crossbar integrated circuit. A crossbar integrated circuit is commonly used to provide a switching capability within a communication device. The communication device can be a component of a switch, a switch fabric, or a router, for example.

The communication processing circuitry (301, 501) in any of the figures 3-7 receives an incoming communication over a serial communication link (311) and transfers the communication to an appropriate crossbar integrated circuit (302-304, 402, 502, 661-663). The crossbar integrated circuit (302-304, 402, 502, 661-663) switches the communication according to a destination of the communication and transfers the communication back to the communication processing circuitry (301, 501). The communication processing circuitry (301, 501) then transfers the communication on to the destination, wherein the switching performed by the crossbar integrated circuit (302-304, 402, 502, 661-663) routes the communication on to the destination.

The invention uses parallel channels (512, 517) to exchange both the communication data and a clock signal with the crossbar integrated circuits (see page 9, lines 6-10 and page 5, line 22

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to page 6, line 1). This is best shown in FIG. 5, which shows detail of the individual parallel links between the communication processing circuitry (501) and ONE particular crossbar integrated circuit (502). An individual parallel channel transfers communications in multiple parallel bit streams (see page 9, lines 8-10). A communications device can include many such crossbar integrated circuits.

The parallel channel also transfers a clock signal in a separate bit stream that is parallel to the bit streams for the communications. A clock channel extends in parallel from a clock circuitry in the parallel channel interface (IF) 511 of the communication processing circuitry 501 to a clock recovery circuitry in a parallel channel IF 521 of the crossbar integrated circuit 502. The clock recovery circuitry for parallel channels is simpler than that for serial channels. The clock recovery circuitry for a parallel channel is shared by all of the parallel data signals within the parallel channel (see page 9, lines 12-13). Advantageously, the simplification and sharing of the clock recovery circuitry reduces the amount of power and physical space that is required to provide synchronized clocking (see page 9, lines 13-15).

The parallel channels in one embodiment comprise differential signal pairs (see page 10, lines 13-17). A parallel channel 512 in one embodiment includes nine signal pairs of channels (see FIG. 5). Eight of these signal pairs transfer communication data and one of these signal pairs transfers a differential clock signal from the communication processing circuitry (501) to the crossbar integrated circuit (502).

GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

1. Whether claims 21-22, 24, 26-34, and 36-40 are anticipated under 35 U.S.C. § 102(e) by U.S. Patent 6,747,971 (Hughes et al.).

2. Whether dependent claim 23 is obvious under 35 U.S.C. § 103(a) over Hughes in view of Applicant Admitted Prior Art (AAPA).

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3. Whether dependent claims 25 and 35 are obvious under 35 U.S.C. § 103(a) over Hughes in view of U.S. Patent 6,185,221 (Aybay).

ARGUMENT

OUTLINE

I. Summary of the brief on appeal.

II. Summary of the requirements for *prima facie* anticipation and obviousness.

III. Discussion of the § 102(e) anticipation rejection of claims 21-22, 24, 26-34, and 36-40.

IV. Discussion of the § 103(a) obviousness rejection of claim 23.

V. Discussion of the § 103(a) obviousness rejection of claims 25 and 35.

I. Summary of the brief on appeal

A. The 35 U.S.C. § 102(e) rejection of claims 21-22, 24, 26-34, and 36-40 is improper because a *prima facie* case for anticipation has not been established, for the following reasons: (1) the cited Hughes reference does not teach or suggest every element of the claims, and (2) the Examiner incorrectly characterizes the Hughes reference.

B. The 35 U.S.C. § 103(a) rejection of claim 23 is improper because a *prima facie* case for obviousness has not been established, for the following reasons: (1) the cited prior art combination does not teach or suggest every element of the claims, and (2) the Examiner incorrectly characterizes the Hughes reference.

C. The 35 U.S.C. § 103(a) rejection of claims 25 and 35 is improper because a *prima facie* case for obviousness has not been established, for the following reasons: (1)

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the cited prior art combination does not teach or suggest every element of the claims, and (2) the Examiner incorrectly characterizes the Hughes reference.

II. Summary of the requirements for *prima facie* indefiniteness, anticipation, and obviousness.

The all elements rule for anticipation is well established over a long series of case law. The all elements rule states that for anticipation to exist, a single anticipating prior art reference must include all elements of a claim. *Hybritech Inc. v. Monoclonal Antibodies, Inc.*, 802 F.2d 1367, 231 USPQ 81 (Fed. Cir. 1986).

To establish a prima facie case of obviousness, the prior art reference (or references when combined) must teach or suggest all the claim limitations. MPEP 2142. *In re Royka*, 490 F.2d 981, 180 USPQ 580 (CCPA 1974). If an independent claim is nonobvious under 35 U.S.C. 103, then any claim dependent therefrom is nonobvious. *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988).

III. Discussion of the § 102(e) anticipation rejection of claims 21-22, 24, 26-34, and 36-40.

Claims 21-22, 24, 26-34, and 36-40 have been finally rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent 6,747,971 (Hughes et al.).

Independent claim 21 requires a plurality of parallel channels between a processing circuitry and each crossbar integrated circuit of a plurality of crossbar integrated circuits. The plurality of parallel channels of a particular crossbar integrated circuit are configured to transfer the communication and a clock signal in parallel to the particular crossbar integrated circuit. Independent claim 31 requires transferring a communication and a clock signal in parallel over a

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plurality of parallel channels to a particular crossbar integrated circuit of a plurality of crossbar integrated circuits. Advantageously, the clock signal is shared by all of the data signals within the parallel channel. The simplification and sharing of the clock circuitry reduces the amount of power and physical space that is required to provide synchronized clocking. The power and space savings can be used to support higher speed communication devices.

The final Office Action is confusing the parallel transmission of signaling overhead in Hughes with the parallel data transmission in the present invention. Hughes transmits signaling information in parallel from an ingress port to ALL crossbar switches. The present invention transmits communication data in parallel from a communication processing circuitry to ONE crossbar integrated circuit of multiple crossbar integrated circuits. Hughes therefore does not anticipate the present invention.

Hughes does not disclose transferring a communication and a clock signal in parallel over a plurality of parallel channels to a particular crossbar integrated circuit of a plurality of crossbar integrated circuits. In contrast, Hughes discloses sending "switch frames" in parallel to multiple switches. Hughes discloses a request controller 314 that sends a switch frame to each switch plane (see col. 6, line 64 to col. 7, line 15). Because the example circuit in FIG. 3 of Hughes has 8 switch planes 309a, 309b, 309c, 309d, 309e, 309f, 309g, and 309h, then as a consequence the switch frame is essentially "broadcast" to eight switch planes.

Hughes does not disclose that a switch plane is transferred in parallel to a particular switch plane of the eight switch planes. Hughes does not disclose that a switch plane is transferred in parallel with a clock signal to a particular switch plane. Hughes does not transmit data in parallel, and only transmits signaling overhead (*i.e.*, a switch frame) in parallel to all crossbar switches.

The final Office Action asserts that Hughes discloses "A plurality of parallel channels between the processing circuitry and each crossbar integrated circuit of the plurality of crossbar integrated circuits . . ." and further asserts that FIG. 3 of Hughes shows parallel links between ingress ports 3204a-n and the switch switching planes 309. This is incorrect. Hughes shows a plurality of links from a particular ingress port to all of the switching planes 309a-309n. Hughes DOES NOT show a plurality of parallel links from the ingress port 304a to the switch 309a, in contrast to the invention.

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The final Office Action further asserts that Hughes transfers a clock signal in parallel, and cites col. 6, line 64 to col. 7, line 15 of Hughes in support of this assertion. Applicant has read the cited text. The cited text merely informs that Hughes transfers service requests to EACH of the switch planes in parallel on a clock tick. Transferring service requests in parallel to each switch plane is not the same as transferring a clock signal in parallel with data from ONE ingress port to ONE switch, as in the present invention.

Applicant points out that the "switch frame" discussed in Hughes at col. 6, line 64 to col. 7, line 15, does not comprise a communication. Hughes discloses that the request controller 314 "constructs a switch frame . . . " and that "Each switch frame contains service requests for selected cells queued in the ingress port." The switch frame therefore comprises internal signaling or overhead data that is constructed in order to operate the system of Hughes. A switch frame is not a communication to be switched.

The final Office Action further asserts that Hughes discloses parallel differential signal pairs as in claim 33 of the invention, and cites col. 5, line 40 to col. 7, line 15 of Hughes in support of this assertion. This is incorrect. Applicant has thoroughly inspected this cited text (and all of Hughes), and does not find any discussion of a parallel channel comprising a pair of differential signal channels.

In the Response to Amendment section of the final Office Action, the Office Action asserts that Hughes discloses parallel channels because Hughes discloses "switch planes 309 in a crossbar arrangement which means there is a channel between every switch plane input and every switch plane output . . . ". Hughes does not teach or suggest that a crossbar switch includes parallel channels. This assertion is simply an assertion without basis.

In the Response to Amendment section of the final Office Action, the Office Action asserts that "Each switch frame contains service requests for selected cells queued in the ingress ports and each ingress port is communicatively coupled to particular switch planes and each switch planes [sic] response [sic] to specific service request on each clock tick. This implies that a switch plane [sic] is transferred in parallel with a clock signal to a particular switch plane." This is incorrect. Hughes states that a switch frame is sent "on a clock tick" and the final Office Action attempts to imply a clock signal transmission into this text. Many electronic circuits can transfer information on a clock tick without also transferring the clock signal. Hughes does not

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state that it transfers a clock signal or a clock data. The implying in the final Office Action is therefore improper and incorrect.

Hughes essentially sends service requests to each switch plane, with the service request detailing the cells that are to be switched (see col. 6, lines 27-40). Each switch plane therefore can perform corresponding switching actions. Applicant cannot understand how this could conceivably relate to transferring data in parallel from ONE ingress port to ONE switch. The text cited by the final Office Action does not teach or suggest transferring data from an ingress port to a switch over parallel channels or transferring a clock signal in parallel with parallel data transmission.

Independent claims 21 and 31 therefore include features that are neither taught nor suggested by Hughes. It is respectfully submitted that a *prima facie* case of anticipation has not been established. As a result, independent claims 21-22, 24, 26-34, and 36-40 are allowable as written. Claims 22, 24, 26-30, 32-34, and 36-40 are dependent on claims 21 and 31. If an independent claim is patentable under 35 U.S.C. 102, then any claim dependent therefrom is also patentable, as a dependent claim includes all of the elements and limitations of the corresponding independent claim.

IV. Discussion of the § 103(a) obviousness rejection of claim 23.

Dependent claim 23 has been finally rejected under 35 U.S.C. § 103(a) as being obvious over Hughes in view of Applicant Admitted Prior Art (AAPA). Dependent claim 23 depends from independent claim 21 and therefore incorporates the limitations of the independent claim. Consequently, claim 23 is patentable for the reasons previously discussed. To establish a prima facie case of obviousness, the prior art reference (or references when combined) must teach or suggest all the claim limitations. MPEP 2142. *In re Royka*, 490 F.2d 981, 180 USPQ 580 (CCPA 1974). If an independent claim is nonobvious under 35 U.S.C. 103, then any claim dependent therefrom is nonobvious. *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988).

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V. Discussion of the § 103(a) obviousness rejection of claims 25 and 35.

Dependent claims 25 and 35 have been finally rejected under 35 U.S.C. § 103(a) as being obvious over Hughes in view of U.S. Patent 6,185,221 (Aybay). Dependent claims 25 and 35 depend from independent claims 21 and 31 and therefore incorporate the limitations of the independent claims. Consequently, claims 25 and 35 are patentable for the reasons previously discussed.

Conclusion

In view of the above, applicant respectfully request that the examiner's rejection of claims 21-40 be reversed.

Respectfully submitted,

Date: 9/1/05

SIGNATURE OF PRACTITIONER

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CLAIMS APPENDIX

21. Communication circuitry comprising:

a processing circuitry configured to receive a communication from a communication link;

a plurality of crossbar integrated circuits; and

a plurality of parallel channels between the processing circuitry and each crossbar integrated circuit of the plurality of crossbar integrated circuits, with the plurality of parallel channels of a particular crossbar integrated circuit being configured to transfer the communication and a clock signal in parallel to the particular crossbar integrated circuit.

22. The communication circuitry of claim 21 wherein the plurality of parallel channels is comprised of parallel differential signal pairs and wherein one of the differential signal pairs is for the clock signal.

23. The communication circuitry of claim 21 wherein the communication link comprises a serial channel.

24. The communication circuitry of claim 21 wherein the communication comprises a data packet.

25. The communication circuitry of claim 21 wherein the communication comprises a fixed-length data packet.

26. The communication circuitry of claim 21 wherein the communication circuitry comprises a switch fabric.

27. The communication circuitry of claim 21 wherein the processing circuitry is comprised of at least one virtual output queue that stores the communication prior to switching and that is associated with an egress port.

28. The communication circuitry of claim 21 wherein the processing circuitry is comprised of at

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least one virtual output queue that stores the communication prior to switching and wherein a virtual output queue is comprised of sub-queues that are each associated with a particular priority.

29. The communication circuitry of claim 21 wherein the processing circuitry is comprised of a multi-cast virtual output queue that stores the communication prior to switching for multi-cast output.

30. The communication circuitry of claim 21 wherein the plurality of parallel channels include multiplexers to perform bit slicing through the crossbar integrated circuits.

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31. A method of operating communication circuitry, the method comprising:

receiving a communication in a processing circuitry from a communication link;

transferring the communication and a clock signal in parallel over a plurality of parallel channels to a particular crossbar integrated circuit of a plurality of crossbar integrated circuits; and

switching the communication in the particular crossbar integrated circuit based on the clock signal.

32. The method of claim 31 wherein transferring the communication and the clock signal in parallel over the plurality of parallel channels comprises transferring the communication and the clock signal over parallel differential signal pairs.

33. The method of claim 31 wherein transferring the communication and the clock signal in parallel over the plurality of parallel channels comprises transferring the communication and the clock signal over parallel differential signal pairs wherein one of the differential signal pairs is for the clock signal.

34. The method of claim 31 wherein the communication comprises a data packet.

35. The method of claim 31 wherein the communication comprises a fixed-length data packet.

36. The method of claim 31 wherein the communication circuitry comprises a switch fabric.

37. The method of claim 31 further comprising, in the processing circuitry, storing the communication in a virtual output queue that is associated with an egress port prior to switching.

38. The method of claim 31 further comprising, in the processing circuitry, storing the communication in a virtual output sub-queue that is associated with a particular priority.

39. The method of claim 31 further comprising, in the processing circuitry, storing the

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communication in a multicast virtual output queue that stores the communication prior to switching for multi-cast output.

40. The method of claim 31 wherein transferring the communication and the clock signal in parallel comprises multiplexing the communications to perform bit slicing through the crossbar integrated circuits.

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EVIDENCE APPENDIX

None

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RELATED PROCEEDINGS APPENDIX

None

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